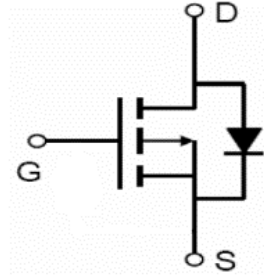


Features

- High density cell design for ultra low $R_{DS(ON)}$
- Fully characterized avalanche voltage and current
- Excellent package for good heat dissipation
- Halogen free
- Qualified to AEC-Q101 standards for high reliability

HF

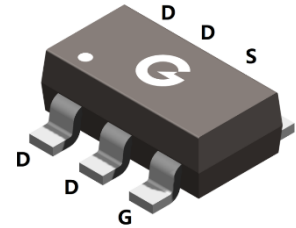


Typical Applications

- Power switching application
- Hard switched and high frequency circuits
- Uninterruptible power supply

Mechanical Data

- Case: SOT-23-6L
- Molding Compound: UL Flammability Classification Rating 94V-0
- Terminals: Matte tin-plated leads; solderability-per MIL-STD-202, Method 208



SOT-23-6L

Ordering Information

Part Number	Package	Shipping Quantity	Marking Code
TBL4P06B-6L	SOT-23-6L	3000 pcs / Tape & Reel	4P06B

Maximum Ratings (@ $T_A = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Value	Unit
Drain-to-Source Voltage	V_{DS}	-60	V
Gate-to-Source Voltage	V_{GS}	± 20	V
Continuous Drain Current ($T_C = 25^\circ\text{C}$)	I_D	-4	A
Continuous Drain Current ($T_A = 25^\circ\text{C}$) *1		-2.5	A
Continuous Drain Current ($T_A = 70^\circ\text{C}$) *1		-2	A
Pulsed Drain Current ($t_p = 10\mu\text{s}$, $T_A = 25^\circ\text{C}$)	I_{DM}	-20	A
Single Pulse Avalanche Energy *3	E_{AS}	14	mJ
Power Dissipation ($T_C = 25^\circ\text{C}$)	P_D	3.5	W
Power Dissipation ($T_A = 25^\circ\text{C}$) *1		1.6	W
Operating Junction Temperature Range	T_J	-55 ~ +150	$^\circ\text{C}$
Storage Temperature Range	T_{STG}	-55 ~ +150	$^\circ\text{C}$

Thermal Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit
Thermal Resistance Junction-to-Case	$R_{\theta JC}$	-	28	35	$^{\circ}\text{C/W}$
Thermal Resistance Junction-to-Air ^{*1}	$R_{\theta JA}$	-	70	78	$^{\circ}\text{C/W}$

Electrical Characteristics (@ $T_A = 25^{\circ}\text{C}$ unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
Static Characteristics						
V _{DSS}	Drain-Source Breakdown Voltage	V _{GS} = 0V, I _D = -250μA	-60	-	-	V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = -60V, V _{GS} = 0V	-	-	-1	μA
I _{GSS}	Gate-Body Leakage Current	V _{GS} = ±20V, V _{DS} = 0V	-	-	±100	nA
On Characteristics						
R _{DS(ON)}	Drain-Source On-resistance ^{*2}	V _{GS} = -10V, I _D = -4A	-	122	170	mΩ
		V _{GS} = -4.5V, I _D = -2A	-	151	200	mΩ
V _{GS(th)}	Gate Threshold Voltage	V _{DS} = V _{GS} , I _D = -250μA	-1	-1.8	-3	V
R _G	Gate Resistance	V _{GS} = 0V, f = 1MHz	-	8.4	-	Ω
Dynamic Characteristics						
C _{ISS}	Input Capacitance	V _{GS} = 0V V _{DS} = -30V f = 1.0MHz	-	402	-	pF
C _{OSS}	Output Capacitance		-	35	-	
C _{RSS}	Reverse Transfer Capacitance		-	27	-	
Switching Characteristics						
t _{d(ON)}	Turn-on Delay Time ^{*4}	V _{DD} = -30V V _{GS} = -10V R _G = 3Ω I _D = -4A	-	7	-	ns
t _r	Turn-on Rise Time ^{*4}		-	3	-	
t _{d(OFF)}	Turn-Off Delay Time ^{*4}		-	28	-	
t _f	Turn-Off Fall Time ^{*4}		-	5.5	-	
Q _G	Total Gate-Charge	V _{DD} = -30V I _D = -4A V _{GS} = -10V	-	11	-	nC
Q _{GS}	Gate to Source Charge		-	2	-	
Q _{GD}	Gate to Drain (Miller) Charge		-	2	-	
Source-Drain Diode Characteristics						
V _{SD}	Diode Forward Voltage ^{*2}	I _{SD} = -4A, V _{GS} = 0V	-	-0.9	-1.2	V
t _{rr}	Reverse Recovery Time	I _{SD} = -4A, V _{GS} = 0V di/dt = 100A/μs	-	26	-	ns
Q _{rr}	Reverse Recovery Charge		-	22	-	nC

Notes:

1. The data tested by surface mounted on a 1 inch² FR-4 board with 20Z copper
2. The data tested by pulsed, pulse width $\leq 300\mu\text{s}$, duty cycle $\leq 2\%$
3. The E_{AS} data shows Max. rating. The test condition is $V_{DD} = -30\text{V}$, $V_{GS} = -10\text{V}$, $L = 0.5\text{mH}$
4. Guaranteed by design, not subject to production

Ratings and Characteristics Curves (@ $T_A = 25^\circ\text{C}$ unless otherwise specified)

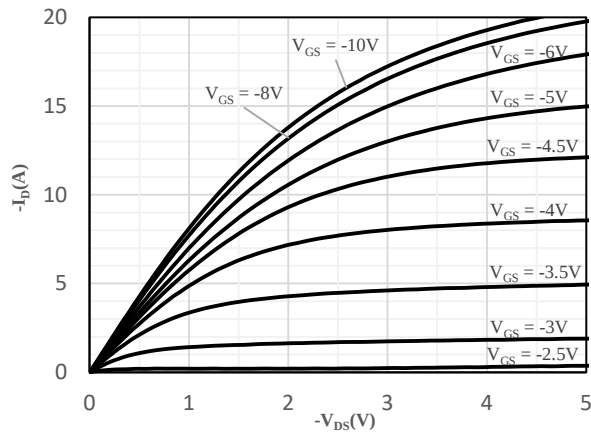


Fig 1 Output Characteristics

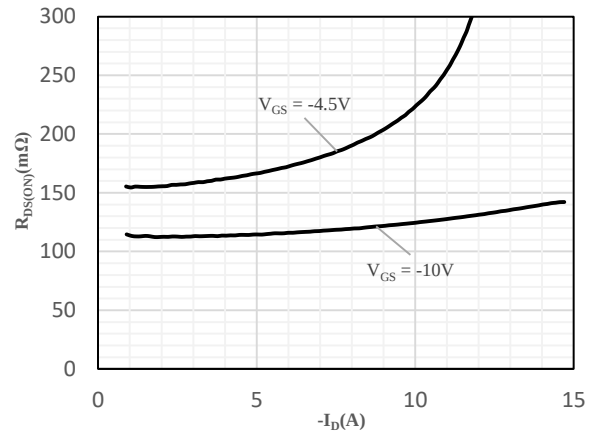


Fig 2 On-Resistance vs. Drain Current and Gate Voltage

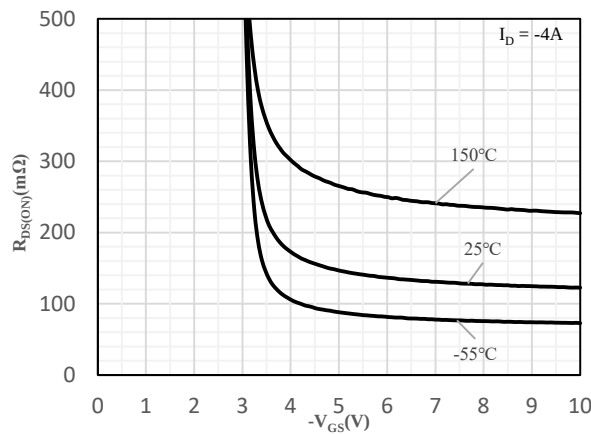


Fig 3 On-Resistance vs. Gate-Source Voltage

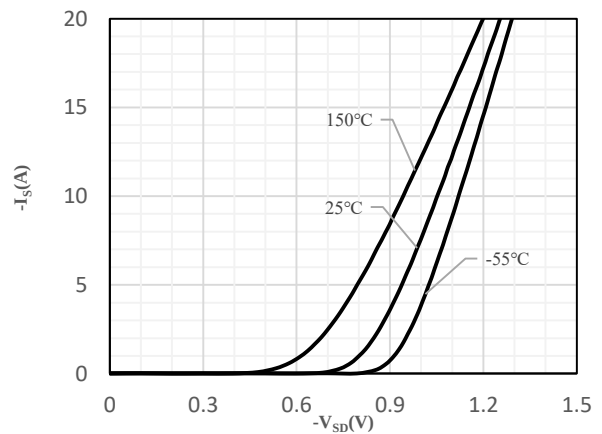


Fig 4 Body-Diode Characteristics

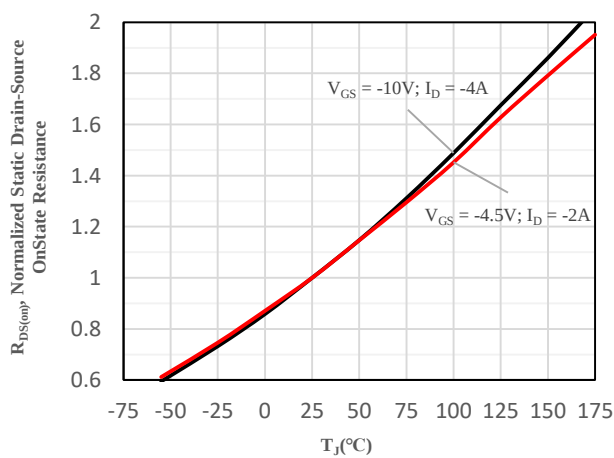


Fig 5 Normalized On-Resistance vs. Junction Temperature

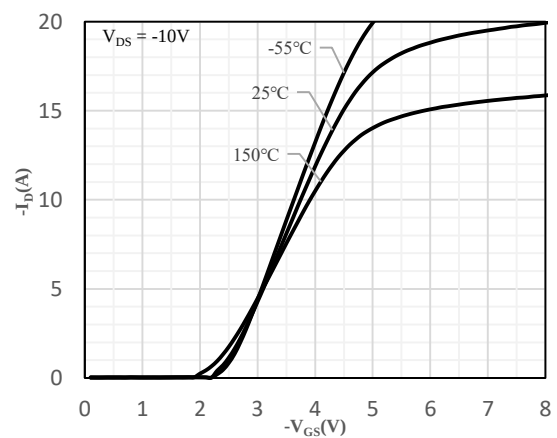


Fig 6 Transfer Characteristics

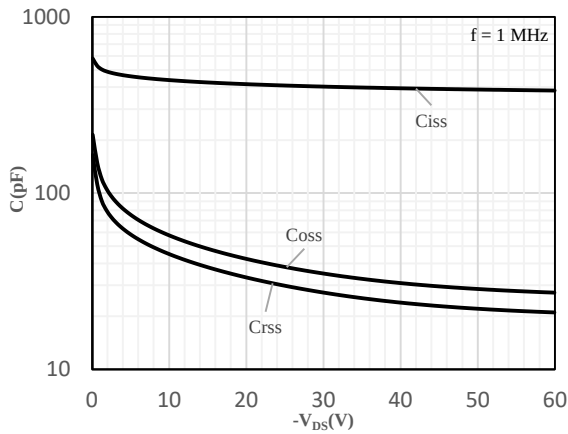


Fig 7 Capacitance Characteristics

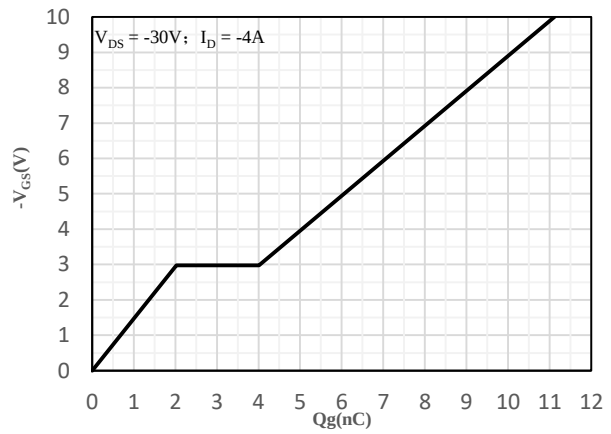


Fig 8 Gate-Charge Characteristics

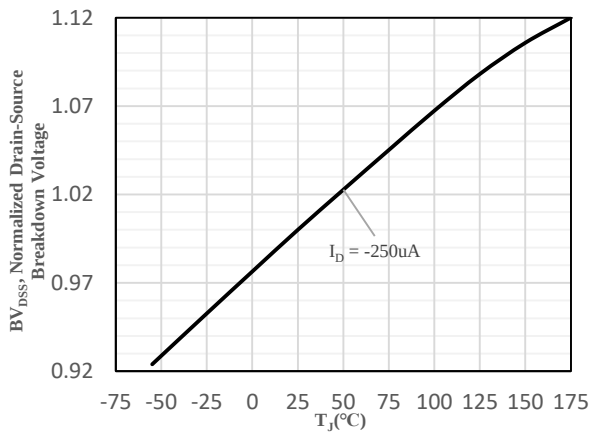


Fig 9 Normalized Breakdown Voltage
vs. Junction Temperature

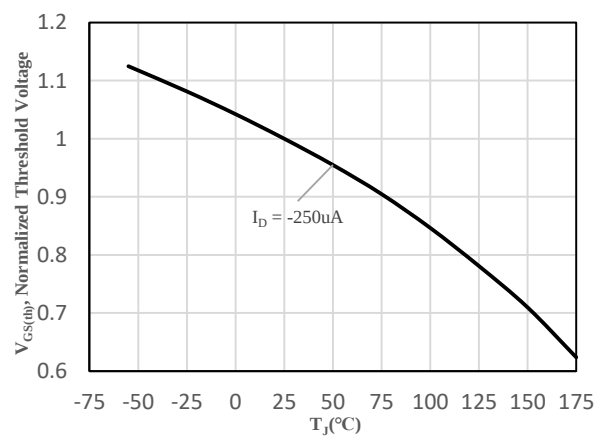


Fig 10 Normalized $V_{GS(th)}$ vs. Junction
Temperature

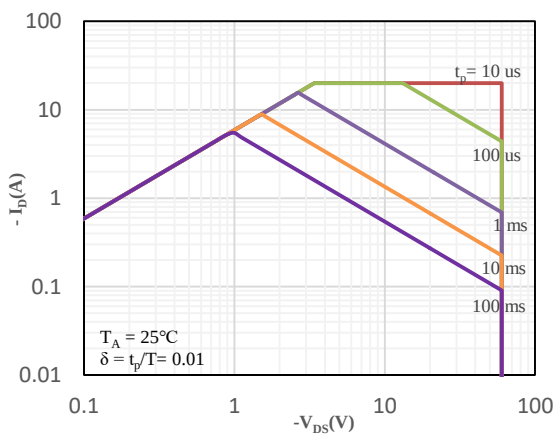


Fig 11 Maximum Safe Operating Area

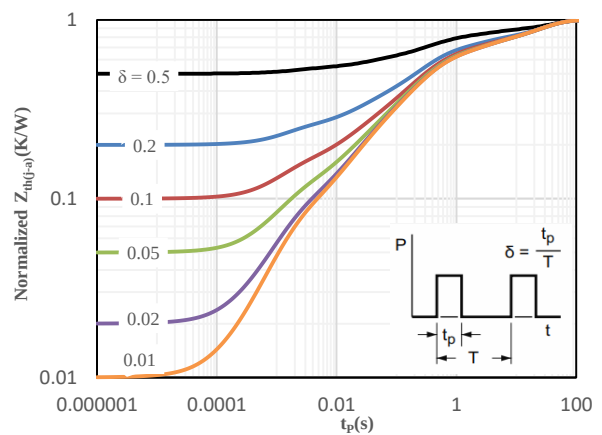
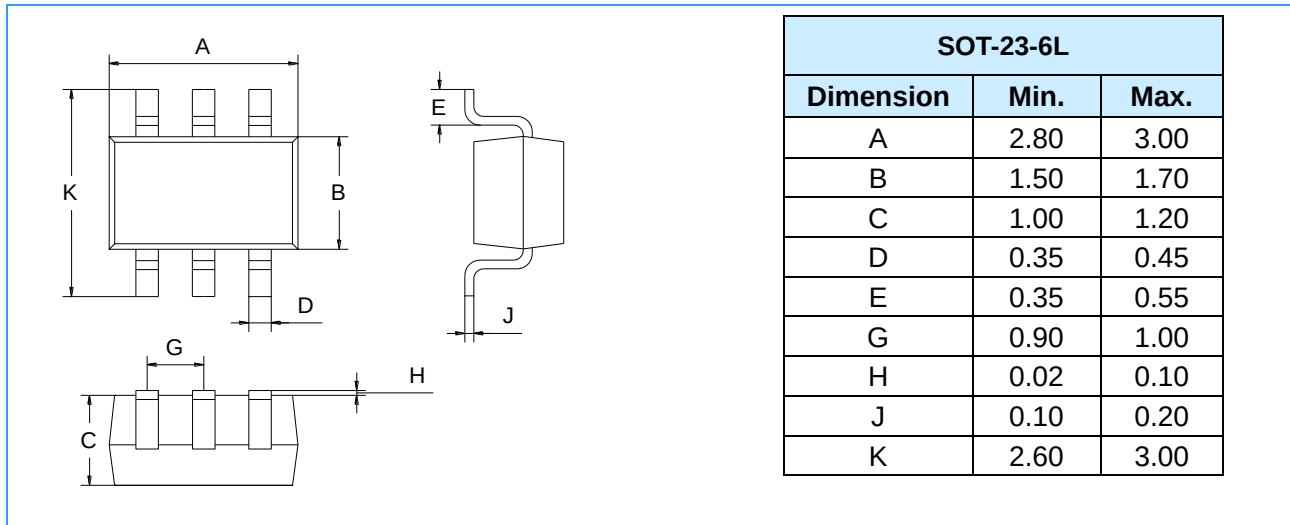


Fig 12 Normalized Transient Thermal Impedance

Package Outline Dimensions (Unit: mm)



Mounting Pad Layout (Unit: mm)



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