

Features

- Low power loss by high speed switching and low on-resistance
- Excellent thermal behavior
- HBM: JESD22-A114-B: 1A
- Product validation acc. JEDEC Standard

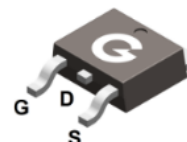
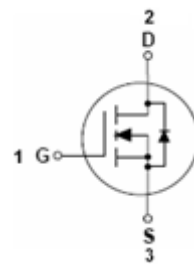
HF

APPLICATIONS

- PFC power supply stages
- Lighting applications
- UPS

Mechanical Data

- Case: TO-252
- Molding Compound: UL Flammability Classification Rating 94V-0
- Terminals: Matte tin-plated leads; solderability-per MIL-STD-202, Method 208



TO-252

Ordering Information

Part Number	Package	Shipping Quantity	Marking Code
SJ65R650D	TO-252	80 pcs / Tube & 2500 pcs / Tape & Reel	SJ65R650D

Maximum Ratings (@ $T_c = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Value	Unit
Drain-to-Source Voltage	V_{DS}	650	V
Gate-to-Source Voltage	V_{GS}	± 30	V
Continuous Drain Current ($T_c = 25^\circ\text{C}$)	I_D	7.5	A
Continuous Drain Current ($T_c = 100^\circ\text{C}$)		4.7	A
Pulsed Drain Current ($t_p = 10\mu\text{s}$, $T_c = 25^\circ\text{C}$)	I_{DM}	30	A
Single Pulse Avalanche Energy ^{*3}	E_{AS}	125	mJ
Power Dissipation ($T_c = 25^\circ\text{C}$)	P_D	63	W
Operating Junction Temperature Range	T_J	$-55 \sim +150$	$^\circ\text{C}$
Storage Temperature Range	T_{STG}	$-55 \sim +150$	$^\circ\text{C}$

Thermal Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit
Thermal Resistance Junction-to-Case	$R_{\theta JC}$	-	1.6	2	$^\circ\text{C/W}$
Thermal Resistance Junction-to-Air ^{*1}	$R_{\theta JA}$	-	50	62	$^\circ\text{C/W}$

Electrical Characteristics (@ $T_A = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
Static Characteristics						
V _{DSS}	Drain-Source Breakdown Voltage	V _{GS} = 0V, I _D = 250μA	650	-	-	V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = 650V, V _{GS} = 0V	-	-	1	μA
I _{GSS}	Gate-Body Leakage Current	V _{GS} = ±30V, V _{DS} = 0V	-	-	±100	nA
On Characteristics						
R _{DS(ON)}	Drain-Source On-resistance *2	V _{GS} = 10V, I _D = 4A	-	0.6	0.65	Ω
V _{GS(th)}	Gate Threshold Voltage	V _{DS} = V _{GS} , I _D = 250μA	2	3	4	V
R _G	Gate Resistance	V _{GS} = 0V, f = 1MHz	-	4.6	-	Ω
Dynamic Characteristics						
C _{ISS}	Input Capacitance	V _{GS} = 0V V _{DS} = 40V f = 250kHz	-	444	-	pF
C _{OSS}	Output Capacitance		-	36	-	
C _{RSS}	Reverse Transfer Capacitance		-	1.1	-	
Switching Characteristics						
t _{d(ON)}	Turn-on Delay Time *4	V _{DD} = 400V V _{GS} = 13V I _D = 3.2A	-	5.3	-	ns
t _r	Turn-on Rise Time *4		-	20.5	-	
t _{d(OFF)}	Turn-Off Delay Time *4		-	23	-	
t _f	Turn-Off Fall Time *4		-	24	-	
Q _G	Total Gate-Charge	V _{DD} = 480V	-	11.3	-	nC
Q _{GS}	Gate to Source Charge	V _{GS} = 10V	-	2.2	-	
Q _{GD}	Gate to Drain (Miller) Charge	I _D = 4A	-	5.3	-	
Source-Drain Diode Characteristics						
V _{SD}	Diode Forward Voltage *2	I _{SD} = 4A, V _{GS} = 0V	-	0.84	1.2	V
t _{rr}	Reverse Recovery Time	I _F = 4A, V _{GS} = 0V	-	193	-	ns
Q _{rr}	Reverse Recovery Charge	di/dt = 100A/μs	-	1.38	-	μC

Notes:

- The data tested by surface mounted on a minimum recommended FR-4 board
- The data tested by pulsed, pulse width $\leq 300\mu\text{s}$, duty cycle $\leq 2\%$
- The E_{AS} data shows Max. rating. The test condition is $V_{DD} = 100\text{V}, V_{GS} = 15\text{V}, L = 50\text{mH}$
- Guaranteed by design, not subject to production

Ratings and Characteristics Curves (@ $T_A = 25^\circ\text{C}$ unless otherwise specified)

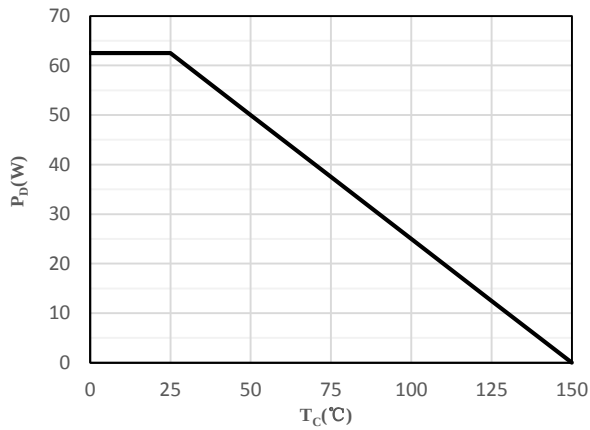


Fig 1 Power Dissipation

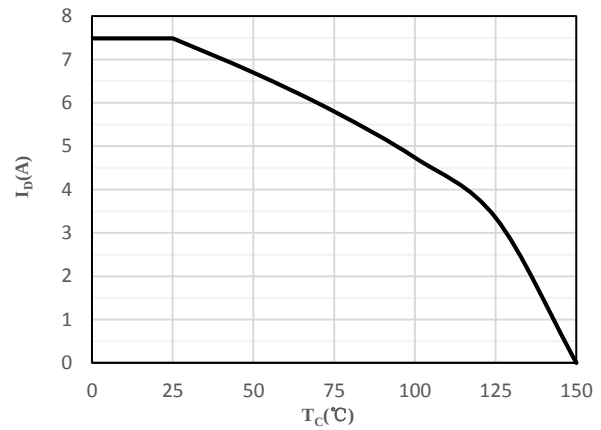


Fig 2 Drain Current

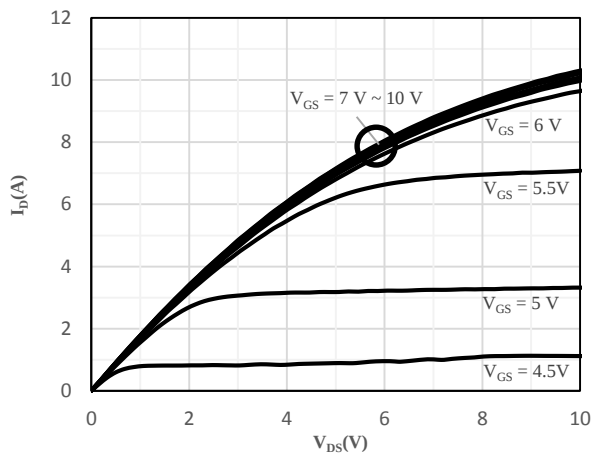


Fig 3 Typical Output Characteristics

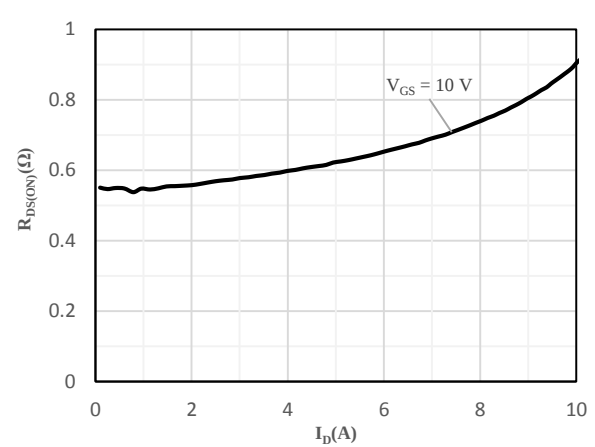


Fig 4 On-Resistance vs. Drain Current
and Gate Voltage

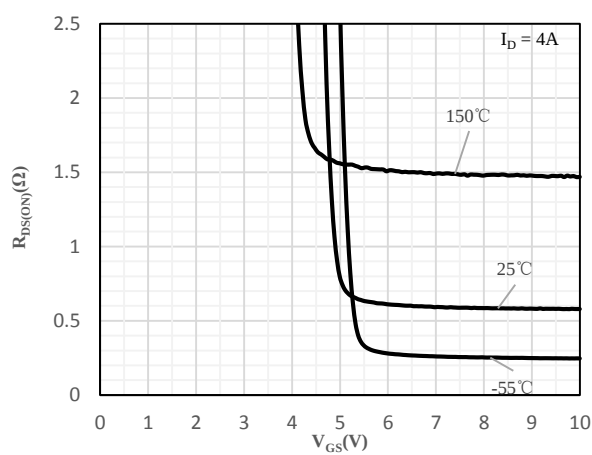


Fig 5 On-Resistance vs. Gate-Source Voltage

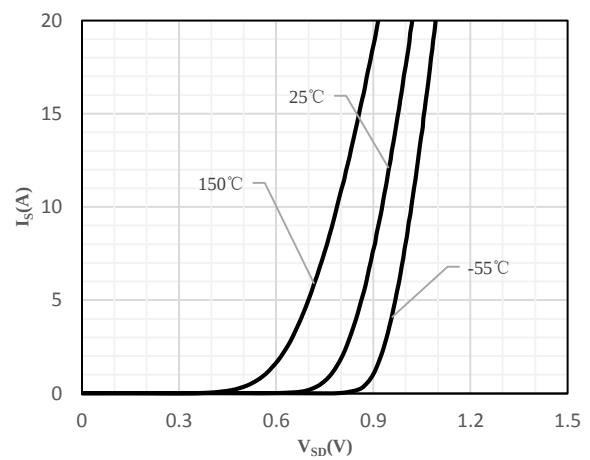


Fig 6 Body-Diode Characteristics

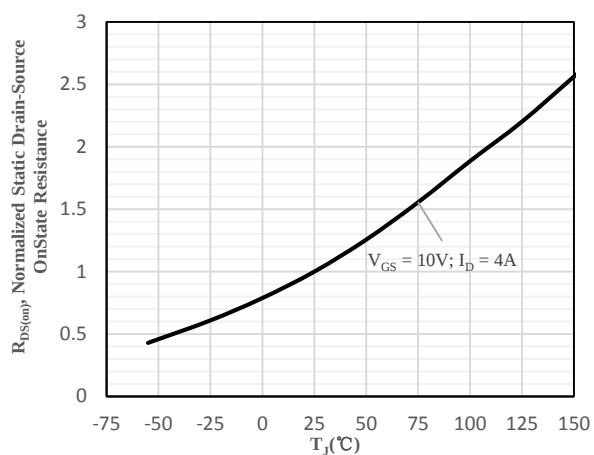


Fig 7 Normalized On-Resistance vs. Junction Temperature

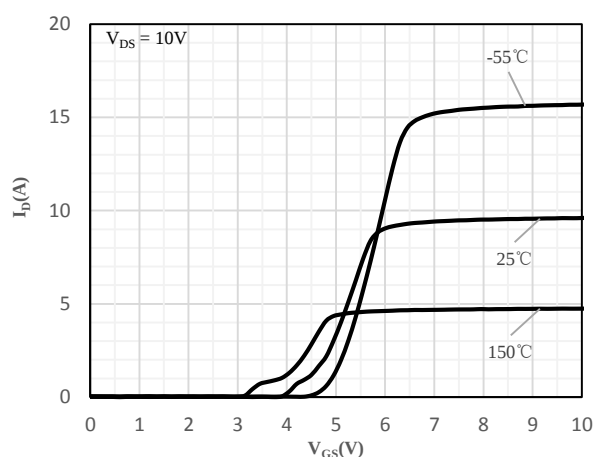


Fig 8 Transfer Characteristics

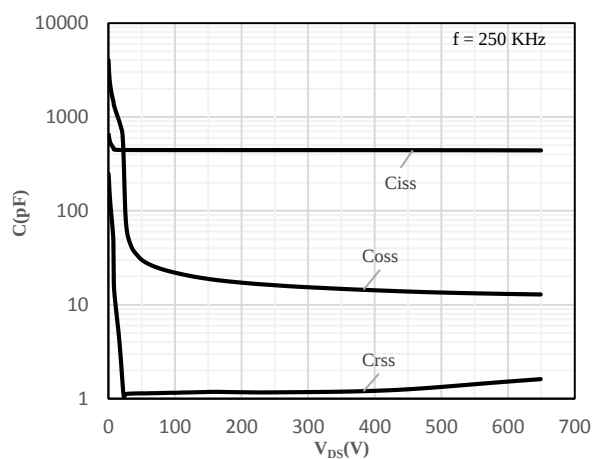


Fig 9 Capacitance Characteristics

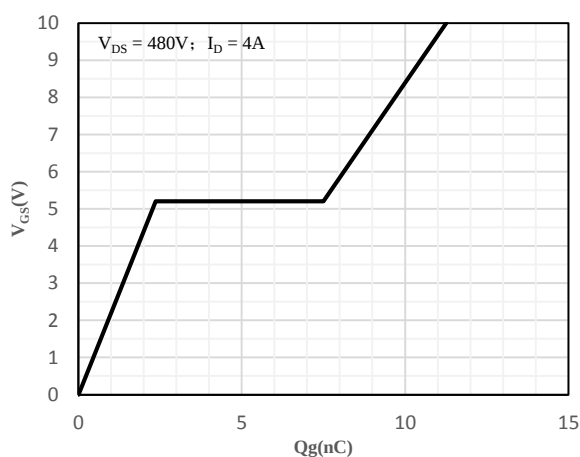


Fig 10 Gate-Charge Characteristics

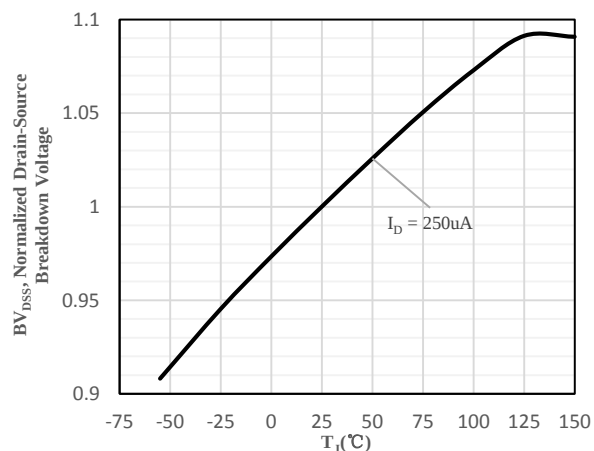


Fig 11 Normalized Breakdown Voltage vs. Junction Temperature

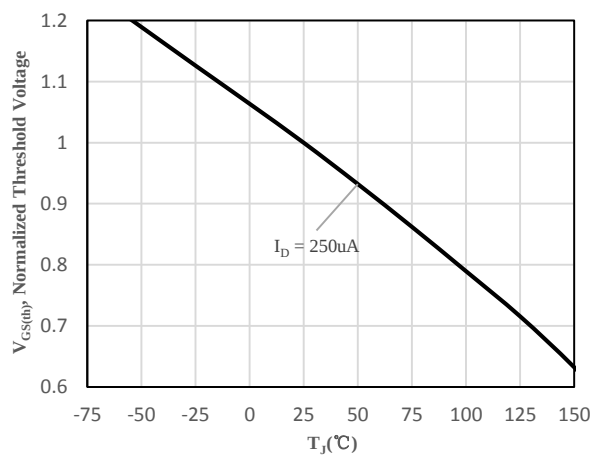


Fig 12 Normalized $V_{GS(th)}$ vs. Junction Temperature

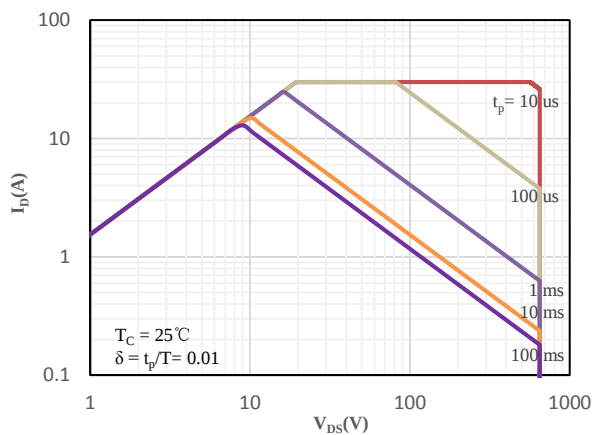


Fig 13 Safe Operation Area

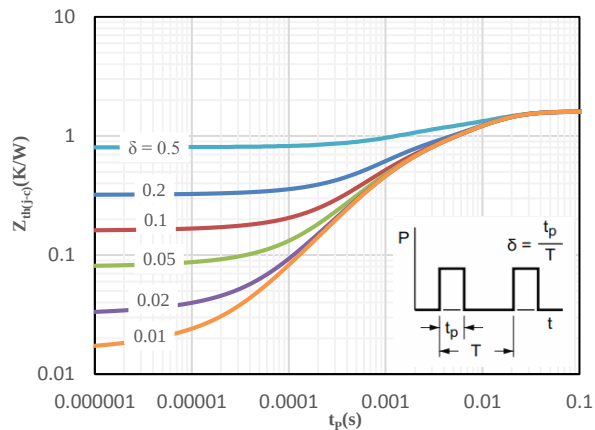
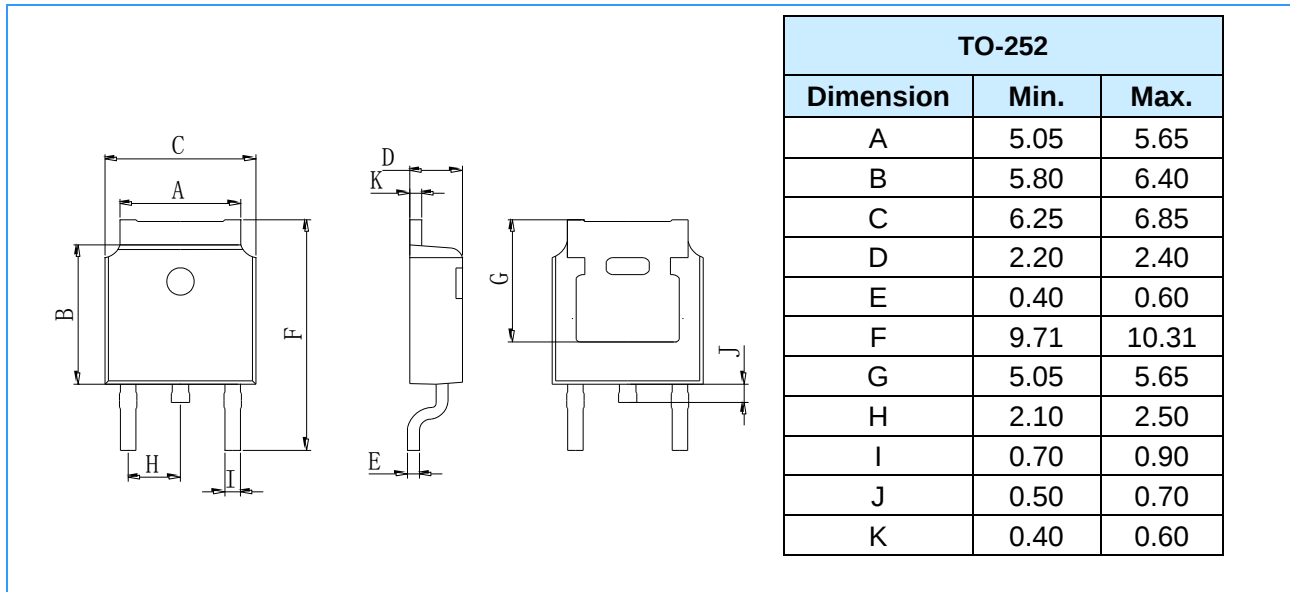
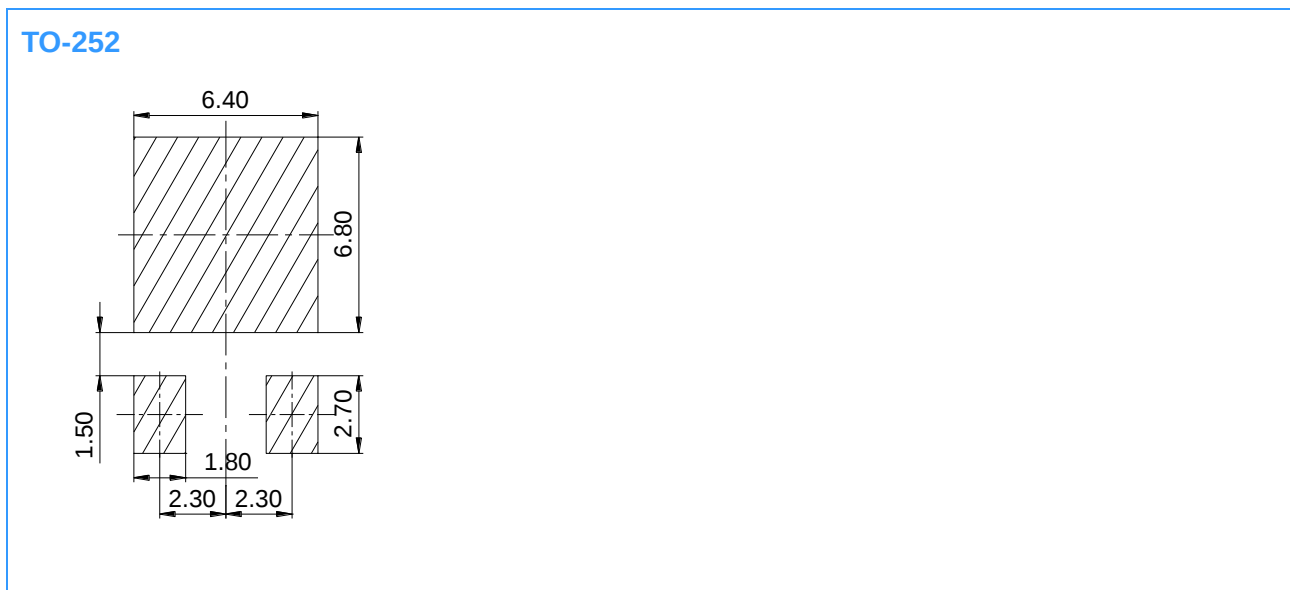


Fig 14 Maximum transient thermal impedance

Package Outline Dimensions (Unit: mm)



Mounting Pad Layout (Unit: mm)



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