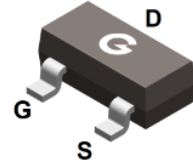
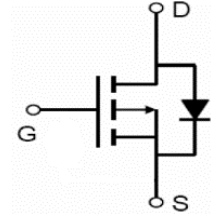


Features

- Super low gate charge
- Excellent C_{dv}/d_t effect decline
- Advanced high cell density Trench technology
- HBM: JESD22-A114-B: 1B
- RoHS compliant with Halogen-free

HF



SOT-23-3L

Mechanical Data

- Case: SOT-23-3L
- Molding Compound: UL Flammability Classification Rating 94V-0
- Terminals: Matte tin-plated leads; solderability-per MIL-STD-202, Method 208

Ordering Information

Part Number	Package	Shipping Quantity	Marking Code
BL450P04-3L	SOT-23-3L	3000 pcs / Tape & Reel	450P04

Maximum Ratings (@ $T_A = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Value	Unit
Drain-to-Source Voltage	V_{DSS}	-40	V
Gate-to-Source Voltage	V_{GSS}	± 20	V
Continuous Drain Current ($T_A = 25^\circ\text{C}$) ^{*1}	I_D	-5.6	A
Continuous Drain Current ($T_A = 70^\circ\text{C}$) ^{*1}		-4.5	A
Pulsed Drain Current ($t_p = 10\mu\text{s}$, $T_A = 25^\circ\text{C}$)	I_{DM}	-40	A
Single Pulse Avalanche Energy ^{*3}	E_{AS}	36	mJ
Power Dissipation ($T_A = 25^\circ\text{C}$) ^{*1}	P_D	2	W
Operating Junction Temperature Range	T_J	-55 ~ +150	$^\circ\text{C}$
Storage Temperature Range	T_{STG}	-55 ~ +150	$^\circ\text{C}$

Thermal Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit
Thermal Resistance Junction-to-Case	$R_{\theta JC}$	-	25	30	$^\circ\text{C/W}$
Thermal Resistance Junction-to-Air ^{*1}	$R_{\theta JA}$	-	55	62	$^\circ\text{C/W}$

Electrical Characteristics (@ $T_A = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
Static Characteristics						
V _{DSS}	Drain-Source Breakdown Voltage	V _{GS} = 0V, I _D = -250μA	-40	-	-	V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = -40V, V _{GS} = 0V	-	-	-1	μA
I _{GSS}	Gate-Body Leakage Current	V _{GS} = ±20V, V _{DS} = 0V	-	-	±100	nA
On Characteristics						
R _{DS(ON)}	Drain-Source On-resistance *2	V _{GS} = -10V, I _D = -5A	-	36	45	mΩ
		V _{GS} = -4.5V, I _D = -3A	-	48	70	mΩ
V _{GS(th)}	Gate Threshold Voltage	V _{DS} = V _{GS} , I _D = -250μA	-1	-1.4	-2.5	V
R _G	Gate Resistance	V _{GS} = 0V, f = 1MHz	-	19	-	Ω
Dynamic Characteristics						
C _{ISS}	Input Capacitance	V _{GS} = 0V V _{DS} = -15V f = 1.0MHz	-	1026	-	pF
C _{OSS}	Output Capacitance		-	96	-	
C _{RSS}	Reverse Transfer Capacitance		-	76	-	
Switching Characteristics						
t _{d(ON)}	Turn-on Delay Time *4	V _{DD} = -15V V _{GS} = -10V I _D = -1A R _G = 3.3Ω	-	19.2	-	ns
t _r	Turn-on Rise Time *4		-	12.8	-	
t _{d(OFF)}	Turn-Off Delay Time *4		-	48.6	-	
t _f	Turn-Off Fall Time *4		-	4.6	-	
Q _G	Total Gate-Charge	V _{DD} = -20V V _{GS} = -4.5V I _D = -2A	-	10.8	-	nC
Q _{GS}	Gate to Source Charge		-	2.8	-	
Q _{GD}	Gate to Drain (Miller) Charge		-	3.2	-	
Source-Drain Diode Characteristics						
V _{SD}	Diode Forward Voltage *2	I _{SD} = -3A, V _{GS} = 0V	-	-0.8	-1.2	V
t _{rr}	Reverse Recovery Time	I _{SD} = -5A, V _{GS} = 0V di/dt = 100A/μs	-	45	-	ns
Q _{rr}	Reverse Recovery Charge		-	19	-	nC

Notes:

- The data tested by surface mounted on a 1 inch² FR-4 board with 2OZ copper
- The data tested by pulsed, pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$
- The E_{AS} data shows Max. rating. The test condition is $V_{DD} = -25V, V_{GS} = -10V, L = 0.5mH$
- Guaranteed by design, not subject to production

Ratings and Characteristics Curves (@ $T_A = 25^\circ\text{C}$ unless otherwise specified)

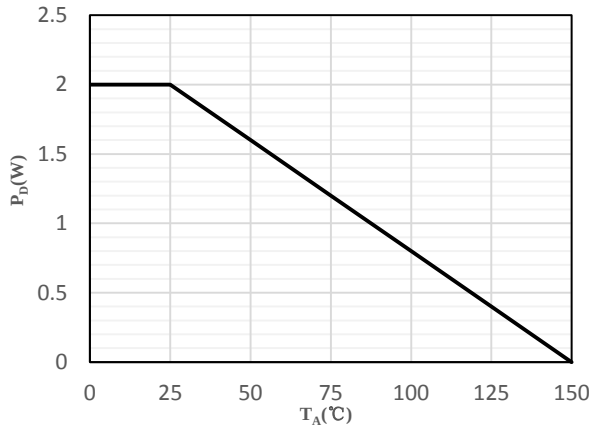


Fig 1 Power Dissipation

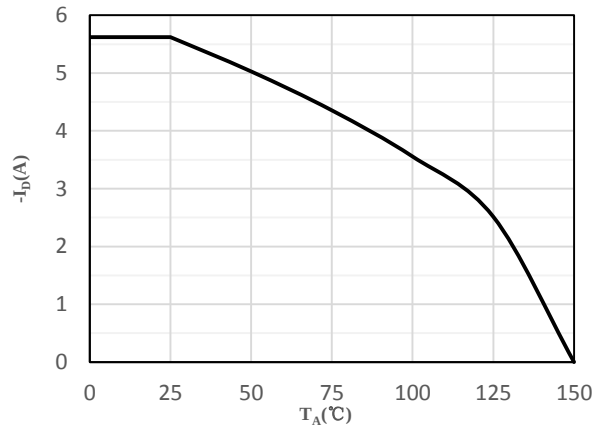


Fig 2 Drain Current

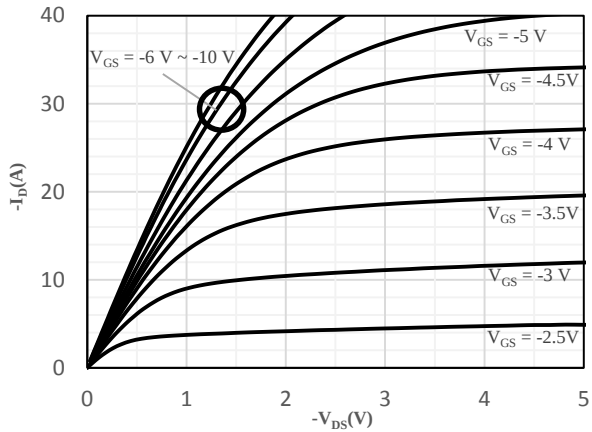


Fig 3 Typical Output Characteristics

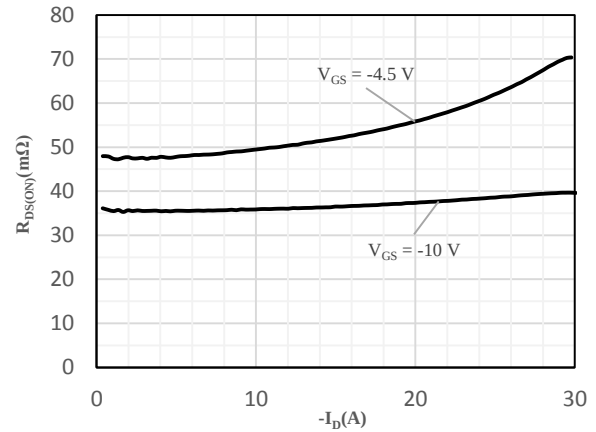


Fig 4 On-Resistance vs. Drain Current
and Gate Voltage

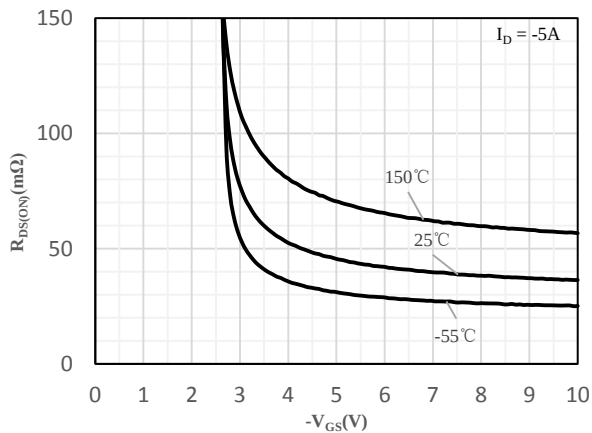


Fig 5 On-Resistance vs. Gate-Source Voltage

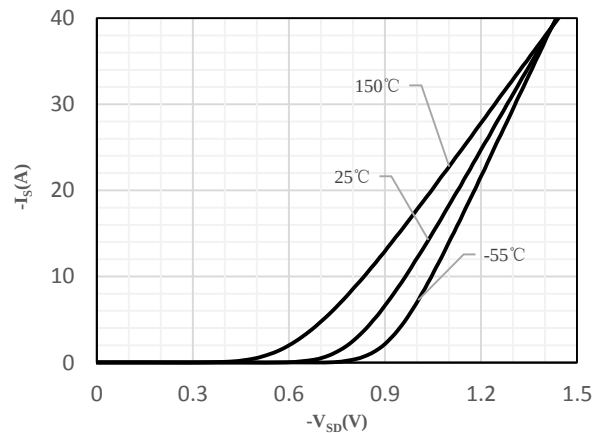


Fig 6 Body-Diode Characteristics

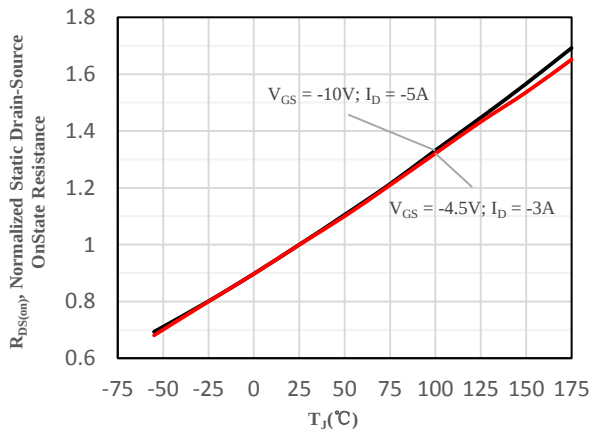


Fig 7 Normalized On-Resistance vs. Junction Temperature

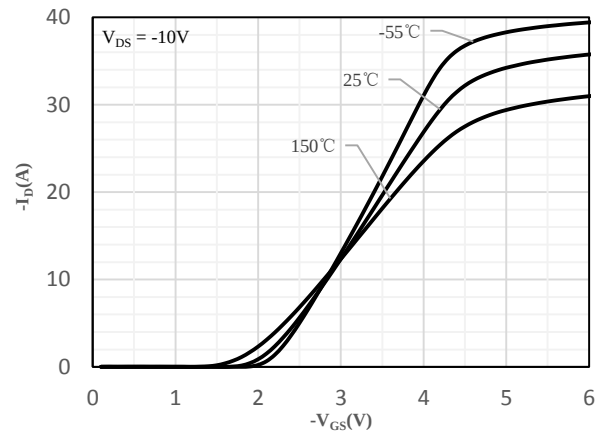


Fig 8 Transfer Characteristics

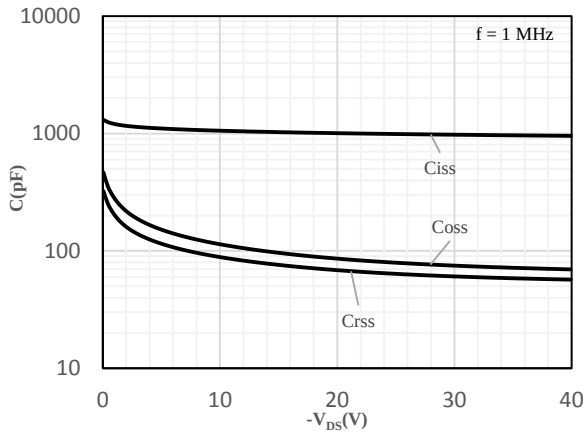


Fig 9 Capacitance Characteristics

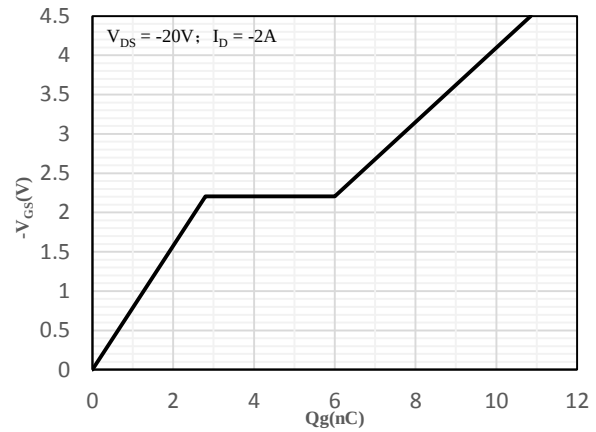


Fig 10 Gate-Charge Characteristics

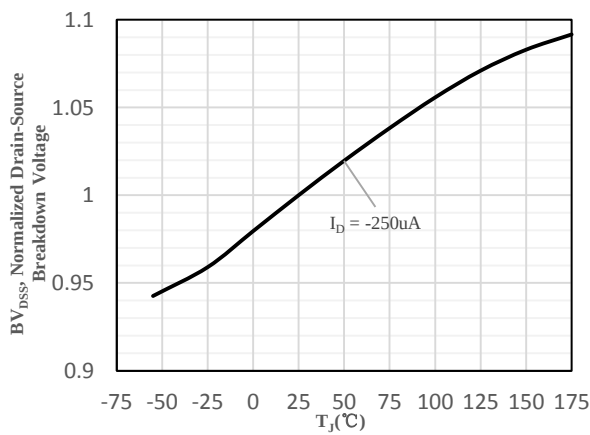


Fig 11 Normalized Breakdown Voltage vs. Junction Temperature

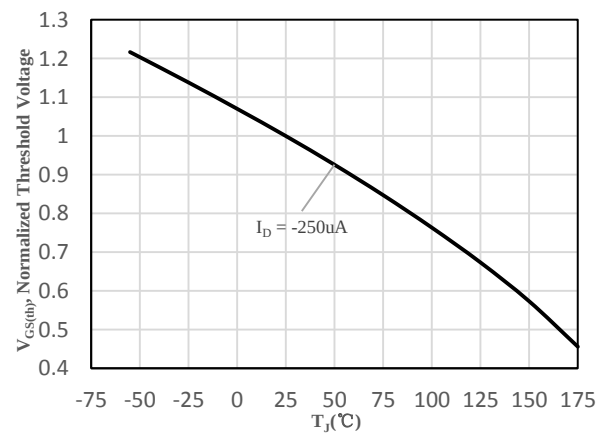


Fig 12 Normalized $V_{GS(th)}$ vs. Junction Temperature

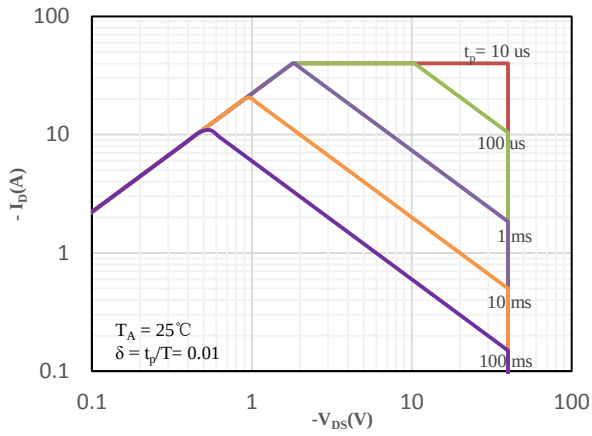


Fig 13 Safe Operation Area

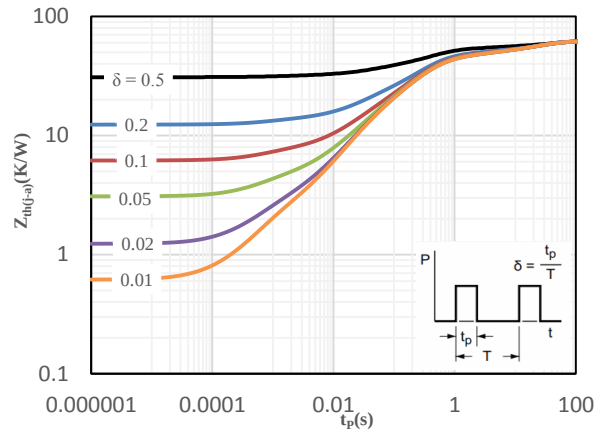
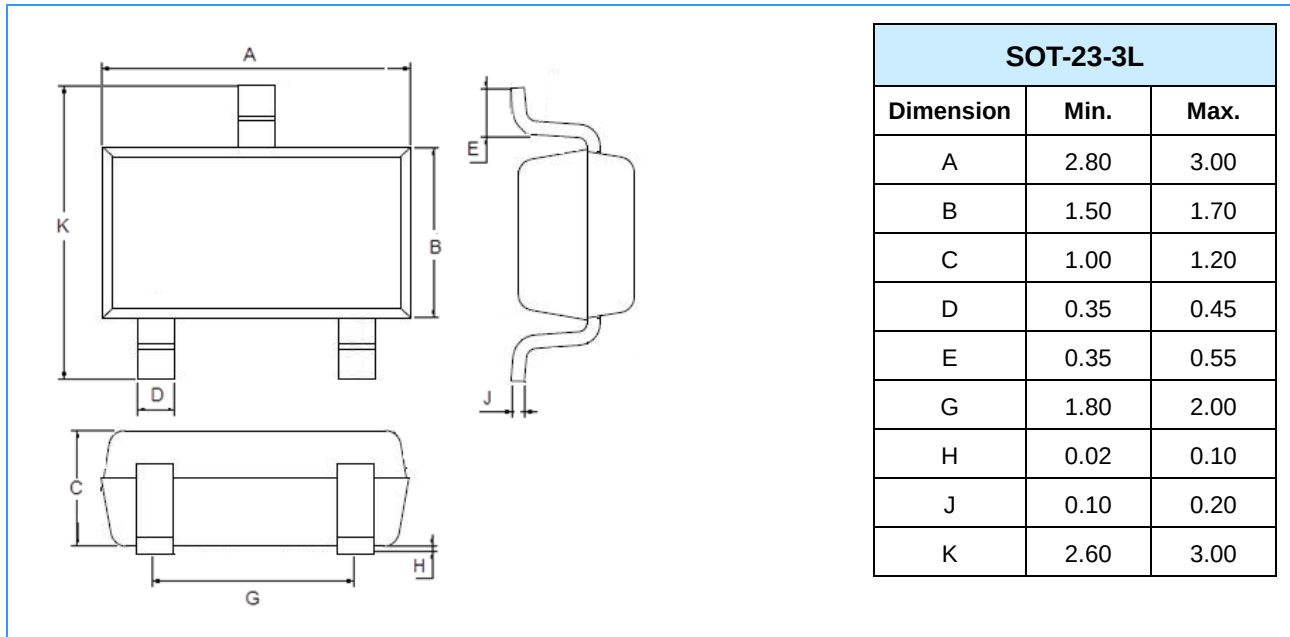


Fig 14 Maximum transient thermal impedance

Package Outline Dimensions (Unit: mm)



Mounting Pad Layout (Unit: mm)

